PATENT
DOCKET NO.: 2207/12002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	John F. Zumkehr
SERIAL NO.	:	10/025,760
FILED	:	December 26, 2001
FOR	:	METHOD AND CIRCUIT TO IMPLEMENT DOUBLE DATA RATE TESTING
GROUP ART UNIT	:	2133
EXAMINER	:	John J. Tabone, Jr.

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. 1.131

I, John F. Zumkehr, hereby declare the following:

1. I am the sole inventor of the subject matter claimed in U.S. Patent Application Serial No. 10/025,760, filed December 26, 2001 and entitled "METHOD AND CIRCUIT TO IMPLEMENT DOUBLE DATA RATE TESTING."

2. The invention described and claimed in the present application was conceived prior to November 27, 2001. Evidence of this fact is shown in the invention disclosure form attached as Exhibit A hereto, which was prepared and submitted to my employer at the time of the disclosure, Intel Corporation, prior to November 27, 2001.

3. I exercised diligence in, at a minimum, constructively reducing the claimed invention to practice from at least a time prior to November 27, 2001 continuously up to December 26, 2001, the date on which the above-cited non-provisional patent application was filed. During that time, I provided information to patent counsel for preparation of the application, and reviewed/revised drafts of the application that was filed on December 26, 2001.

I, John F. Zumkehr, acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the above-cited non-provisional patent application or any patent issuing thereon. Likewise, I declare under penalty of perjury that the above statements are true and correct to the best of my knowledge, information and belief.

Respectfully submitted,

Dated: 11/1/2004

John F. Zumkehr

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INTEL INVENTION DISCLOSURE

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

located at http://legal.intel.com

DATE: _____ ARCHITECTURE COMM. / IAG / EPG / ECD

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed and signed, please return this form to the **Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval.** If you have any questions, please call **264-0444.**

1. Inventor: Zumkehr (Last Name) John (First Name) F. (Middle Initial)

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*If you are unsure of this information, please discuss with your manager.

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PATENT DATABASE GROUP
INTEL LEGAL TEAM

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INV'

2. Title of Invention: Method to Implement DDR Setup and Hold Testing on Die

3. What technology/product/process (code name) does it relate to (be specific if you can):
   Cayuse

4. Include several key words to describe the technology area of the invention in addition to # 3 above: DDR, source synchronous, calibration, PC266, PC333

5. Stage of development (i.e. % complete, simulations done, test chips if any, etc.): micro architecture stage of development

6. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

   NO: X YES: _____ If YES, was the manuscript submitted for pre-publication approval? _____

   IDENTIFY THE PUBLICATION AND THE DATE PUBLISHED: _____

   (b) Has your invention been used/sold or planned to be used/sold by Intel or others?

   NO: X YES: _____ DATE WAS OR WILL BE SOLD: _____

ATTY - SEE ATTACHED RELATED APPLN

I have read and understand this invention: _____ Date: _____

(c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?

NO: X YES: _____ Name of SIG/Standard/Specification: _____

(d) If the invention is embodied in a semiconductor device, actual or anticipated date of tapeout? _____

(e) If the invention is software, actual or anticipated date of any beta tests outside Intel _____

7. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia? NO: X YES: _____ Name of individual or entity: _____

8. Is this invention related to any other invention disclosure that you have recently submitted? If so, please give the title and inventors: _____

_____

PLEASE READ AND FOLLOW THE DIRECTIONS ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION

Please attach a description of the invention to this form and include the following information:

1. Describe in detail what the components of the invention are and how the invention works.

2. Describe advantage(s) of your invention over what is done now.

3. YOU MUST include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.

4. Value of your invention to Intel (how will it be used?).

5. Explain how your invention is novel. If the technology itself is not new, explain what makes it different.

6. Identify the closest or most pertinent prior art that you are aware of.

7. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM
OR FORWARD IT ELECTRONICALLY VIA E-MAIL TO "INVENTION DISCLOSURE SUBMISSION"

DATE: _____ SUPERVISOR: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

I have read and understand this invention: _____ Date: _____

Method to Implement DDR Setup and Hold Testing on Die

Double Data Rate (DDR) devices use a source-synchronous clocking protocol to transfer data from the memory to the memory controller using SSTL_2 signaling levels. Data (DQ) from memory is captured by the memory controller using a clock (DQS) supplied by the memory devices. The DQS from the memory devices is delayed by the memory controller to capture the data from the memory devices. Uncertainty in this DQS delay and setup and hold for the capture mechanism adds to the overall setup and hold time for the memory controller.

The setup and hold relationship between DQ and DQS at the memory controller needs to become smaller and smaller as DDR memory gets faster which presents a problem for testing. External testers have limitation on maintaining tight timing relationships between multiple tester pins due to tester edge placement limitations. These limitations require the tested setup and hold time be relaxed to guarantee that tested parts will meet published specifications. This currently can double the setup and hold times of the memory controller, which reduces the system margins. As memory speeds increase to DDR 266 and DDR 333, the performance of the system cannot be guaranteed.

One solution that has been done on other chipsets and other interfaces, is to incorporate a self-test function on the die which does not depend on the external tester's accuracy to measure setup and hold times. This method is called AC Input/Output (I/O) Loop-back testing in which the test pattern is generated on die, looped through the bi-directional output buffers, received and then compared with the original test pattern. The receive register is clocked with the delayed source-synchronous clock that is programmed with the desired setup and hold parameters for the inputs. Because the pattern is generated on-die, the accuracy of the test pattern is only related to the skew due to clock error for the source synchronous test pattern which can be about 25% or less than that of current testers.

Implementing this scheme is difficult for DDR I/O in that part of the setup and hold on the memory controller is the uncertainty of the delay line used to delay the DQS that captures the DQ. This same delay line that is a large part of the setup/hold measurement must be counted on to test itself. This makes the value of this test degrade because the uncertainty of the delay line, which can be larger than the tester edge placement limitations, is being used to provide accurate testing. In this case, doing AC I/O loop-back would be of no value.

Integrating this method for DDR type I/O presents a problem due to the coincidental nature of DQ and DQS signals. This invention details an innovative way of integrating this technique with DDR I/O to reduce the setup and hold times needed by the microcircuit.

Invention Claims

Our invention claims the following innovations:

(1) System of logic to test setup and hold of DDR capture logic
   - (a) State Machine for performing pattern testing
   - (b) Logic for sending looping patterns through DDR devices for testing
   - (c) Control of clock tree for testing
   - (d) Pattern detection and comparison logic

(2) Logic to control clock trees
   - (a) Clock and clock bar tree
   - (b) Logic to select source of clock for setup and hold testing
   - (c) Delay cell for setup and hold testing

Our invention modifies the clock trees in a novel manner to allow AC I/O loop-back to be incorporated into the memory controller. Pattern generation and checking logic is also included as needed in an AC I/O loop-back type circuit.

Other known methods of performing this setup and hold measurement would require better testers. Assuming that such testers could be purchased, this would be an enormous expense for production lines.

Competitors such as VIA or ServerWorks would be interested in this invention.

Benefit to Intel

The value of this invention is to keep Intel in the lead in DDR memory technology. This invention would be applicable for current DDR chipsets, DDR II, and Quad Data Rate products Intel will be fielding in the future.

I have read and understand this invention: _____ Date: _____

Invention Details

Clock Tree Modification

The memory controller typically has two clock trees to implement the required timing for writes to DDR type memory. One clock tree runs at twice the DDR memory clock rate while the second clock tree is equivalent to the first clock tree except that it is 180 degrees out of phase. This is often called a clock/clock bar implementation. The advantage of the clock/clock bar implementation is that precise control of timing on a half-clock period basis can be done. This is important for DDR writes where DQS and DQ must occur on a half-period interval.

However, when generating AC I/O loop-back patterns, these two clock trees must be in phase for the normal read test case. To handle this, the clock generation logic needs to operate these two clock trees in two modes: in phase and 180 degrees out of phase.

In the test mode with the clock/clock bar being generated in phase, an additional modification needs to be made to test setup and hold times. A delay element calibrated for the setup/hold test value needs to be inserted into the appropriate clock tree generation logic to do setup/hold testing. This delay element is calibrated before the testing phase.

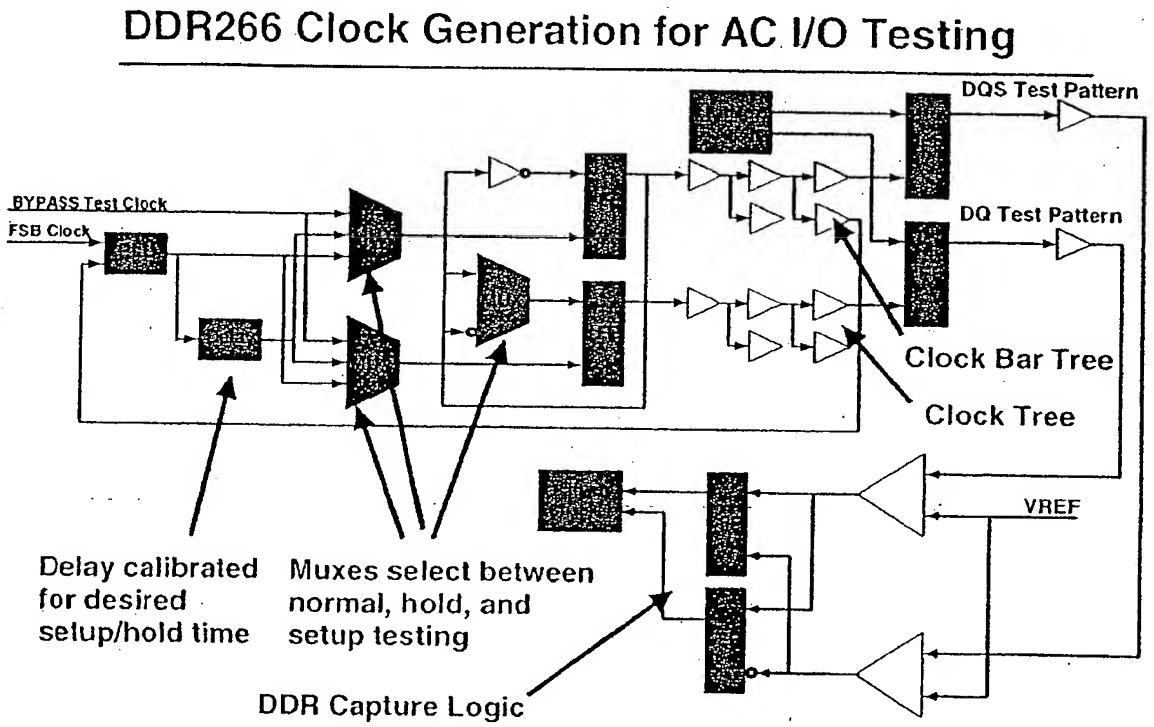

Figure 1: Clocking Plan for DDR Self Testing

Pattern Generation and Checking Logic

Pattern generation logic is connected to the DQ/DQS output logic of the memory controller so that the appropriate test patterns can be outputted. On the receiver end of the DDR I/O cell, a pattern checker is connected to verify the proper data capture. If the received pattern does not match the expected pattern, an error is indicated in the test.

State Machine Logic

A state machine is included in the memory controller to sequence the pattern generation and checking .

I have read and understand this invention: _____ Date: _____